AMENDMENTS TO THE CLAIMS

This listing of claims supersedes all prior versions and listings of claims in this application:

LISTING OF CLAIMS:

1. *(Currently Amended)* A heterojunction field effect type semiconductor device, comprising:

a GaAs substrate;

a channel layer formed over said GaAs substrate;

a first semiconductor layer including no aluminum formed over said channel layer;

a cap layer of a first conductivity type formed on said first semiconductor layer, said cap layer creating a first recess on said first semiconductor layer;

first and second ohmic electrodes formed on said cap layer;

a second semiconductor layer of a second conductivity type formed on said first semiconductor layer within said first recess, said second semiconductor layer being isolated from said cap layer;

a gate electrode formed on said second semiconductor layer; and

a third semiconductor layer made of GaAs/AlGaAs interposed between said first semiconductor layer, wherein said third semiconductor layer comprises an GaAs layer formed on said AlGaAs layer, and said cap layer and having a second recess,

said second semiconductor layer passing through the second recess of said third semiconductor layer to reach said first semiconductor layer.

2. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said channel layer comprises an undoped InGaAs layer.

3. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said channel layer comprises a GaAs layer of said first conductivity type.

4. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said first semiconductor layer comprises an undoped GaAs layer.

5. *(Previously Presented)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein each of said cap layer comprises a GaAs layer.

6. *(Previously Presented)* The heterojunction field effect type semiconductor device as set forth in claim 1, further comprising a wide recess etching stopper layer of said first conductivity type beneath said cap layer.

7. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 6, wherein said wide recess etching stopper layer comprises an AlGaAs layer.

8. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 6, wherein said wide recess etching stopper layer comprises an InGaP layer.

9. *(Cancelled)*

10. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said second semiconductor layer comprises a GaAs layer.

11. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said second semiconductor layer comprises an AlGaAs layer.

12. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said second semiconductor layer comprises an InGaP layer.

13. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said cap layer comprises:

an $In_xGa_{1-x}As$ ($0 \leqq x<0.5$) cap layer; and

an $In_{0.5}Ga_{0.5}As$ cap layer formed on said $In_xGa_{1-x}As$ cap layer,

said device further comprising an InGaP wide recess etching stopper layer of said first conductive type beneath said $In_xGa_{1-x}As$ cap layer.

14. *(Cancelled)*

15. *(Previously Presented)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said third semiconductor layer has a thickness of more than 5nm.

16. *(Previously Presented)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said third semiconductor layer comprises:

an undoped AlGaAs layer; and

an undoped GaAs layer formed on said undoped AlGaAs layer.

17. *(Original)* The heterojunction field effect type semiconductor device as set forth in claim 16, wherein said first semiconductor layer is of said first conductivity type.

18. *(Previously Presented)* The heterojunction field effect type semiconductor device as set forth in claim 1, wherein said third semiconductor layer comprises:

an AlGaAs layer of said first conductivity type; and

an undoped GaAs layer formed on said AlGaAs layer.

19. *(Withdrawn)* A method for manufacturing a heterojunction field effect type semiconductor device, comprising:

growing at least a channel layer, a first semiconductor layer including no aluminum, a wide recess etching stopper layer of a first conductivity type, and a cap layer of said first conductivity type over a GaAs substrate by a first epitaxial growth process;

selectively removing said cap layer by using said wide recess etching stopper layer as a stopper to create a first recess within said cap layer;

depositing an insulating layer on the entire surface after said first recess is created;

perforating said insulating layer to expose said first semiconductor layer;

growing a second semiconductor layer of a second conductivity type by a second epitaxial growth process, so that said second semiconductor layer is buried in said first recess and contacts said first semiconductor layer;

forming a gate electrode on said second semiconductor layer; and

forming ohmic electrodes on said cap layer.

20. *(Withdrawn)* The method as set forth in claim 19, wherein said channel layer comprises an undoped InGaAs layer.

21. *(Withdrawn)* The method as set forth in claim 19, wherein said channel layer comprises a GaAs layer of said first conductivity type.

22. *(Withdrawn)* The method as set forth in claim 19, wherein said first semiconductor layer comprises an undoped GaAs layer.

23. *(Withdrawn)* The method as set forth in claim 19, wherein said cap layer comprises a GaAs layer.

24. *(Withdrawn)* The method as set forth in claim 19, wherein said wide recess etching stopper layer comprises an AlGaAs layer.

25. *(Withdrawn)* The method as set forth in claim 19, wherein said wide recess etching stopper layer comprises an InGaP layer.

26. *(Withdrawn)* The method as set forth in claim 19, further comprising partly removing said wide recess etching stopper layer in self-alignment with said cap layer after said first recess is created.

27. *(Withdrawn)* The method as set forth in claim 19, wherein said second semiconductor layer comprises a GaAs layer.

28. *(Withdrawn)* The method as set forth in claim 19, wherein said second semiconductor layer comprises an AlGaAs layer.

29. *(Withdrawn)* The method as set forth in claim 19, wherein said second semiconductor layer comprises an InGaP layer.

30. *(Withdrawn)* The method as set forth in claim 19, wherein said cap layer comprises:

an $In_xGa_{1-x}As$ ($0 \leqq x<0.5$) cap layer; and

an $In_{0.5}Ga_{0.5}As$ cap layer formed on said $In_xGa_{1-x}As$ cap layer,

said device further comprising an InGaP wide recess etching stopper layer of said first conductive type beneath said $In_xGa_{1-x}As$ cap layer.

31. *(Withdrawn)* The method as set forth in claim 19, further comprising growing a third semiconductor layer interposed between said first semiconductor layer and said cap layer by said first epitaxial growth,

said insulating layer perforating comp rising perforating said third semiconductor layer to create a second recess,

said second semiconductor layer passing through the second recess of said third semiconductor layer to reach said first semiconductor layer.

32. *(Withdrawn)* The method as set forth in claim 31, wherein said third semiconductor layer has a thickness of more than 5nm.

33. *(Withdrawn)* The method as set forth in claim 31, wherein said third semiconductor layer comprises:

an undoped AlGaAs layer; and

an undoped GaAs layer formed on said undoped AlGaAs layer.

34. *(Withdrawn)* The method as set forth in claim 33, wherein said first semiconductor layer is of said first conductivity type.

35. *(Withdrawn)* The method as set forth in claim 31, wherein said third semiconductor layer comprises:

an AlGaAs layer of said first conductivity type; and

an undoped GaAs layer formed on said undoped AlGaAs layer.